New Transmission Line Structure with Suppressed Eddy Current Effects

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Abstract — **A new transmission line structure is presented which features suppression of eddy currents and skin-effect. This results in lower loss and lower frequency dependence of line parameters. Transmission lines were fabricated in a standard digital CMOS process with 3 metal layers and low resistance substrate. Measurements were performed and the successful reduction of eddy currents in the metal conductors could clearly be identified.**

I. Introduction

Transmission lines are basic elements for high frequency circuits. Losses in transmission lines are mainly caused by ohmic losses in the conductors, dielectric losses and eddy currents/skin-effect. In this work, we present a new conductor structure that is based on a new idea to reduce eddy current effects of conductors. The method is patent pending [1]. By applying this method, the current is forced to flow more homogeneously distributed in the conductor cross section at high frequencies.

Several works [2,3] have already dealt with the substrate losses of transmission lines on silicon. Using an epi-wafer with low resistance bulk-substrate, two kinds of substrate losses have to be considered. First, the electric field introduces a capacitively coupled substrate current thru the lossy substrate. This effect can be suppressed by shielding the electric field with a ground plane [2]. A second loss mechanism are eddy currents that are induced in low resistance bulk substrate. To reduce these eddy-currents, the magnetic field that penetrates into the bulk-substrate has to be reduced. This has successfully been demonstrated with coplanar lines with small spacing and line width and with microstrip structures, where the lowest metal layer is used as the ground plane [3].
In this work, to achieve low loss in a standard CMOS technology with low resistance epi-substrate, we use the microstrip line structure to reduce substrate-induced losses and combine this with our new method for the suppression of conductor eddy currents.

II. Method for the Suppression of Conductor Eddy Currents

In the following explanation and discussion, we will not deal separately with skin-effect or proximity-effect, but enclose all these effects in the term eddy currents, because they are all based on the same principles of magnetic interaction. We do however distinguish between eddy currents in the substrate and in the conductor. The invention presented below is capable of suppressing conductor eddy currents.

High frequency magnetic fields accelerate electric charge with an electric field that is proportional to the area that is enclosed by the path of the electric field.

$$\frac{\partial \Phi}{\partial t} = \iint_A \frac{\partial \vec{B}}{\partial t} d\vec{a} = -\oint_P \vec{E} d\vec{p} \qquad (1)$$

Here, Φ is the magnetic flux of $\vec{B}$ through the area A. (see Fig. 1). And $\vec{E}$ is the electric field along its perimeter P. To reduce the electric field with a given magnetic field, we therefore have to reduce the area that is enclosed. This is conventionally done by using thinner conductors, which however increases the DC-resistance. Note that introducing longitudinal slots in a transmission line does not reduce the area, as the connections at the beginning and the end of the line close the path around the area that has been opened with the slot (see Fig. 2) and therefore the situation does not change.

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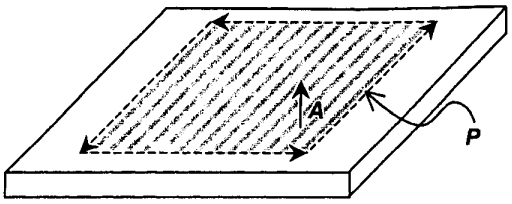


Fig. 1. High frequency magnetic field $\vec{B}$ through area A induces electric field $\vec{E}$ along path P.

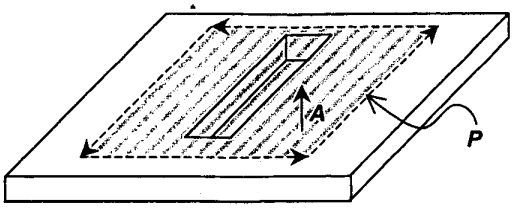


Fig. 2. Longitudinal slots do not reduce Area A and therefore do not reduce the induced Electric Field along P.

However, there is still a possibility to reduce the area. It is based on the fact that the calculation of the area is sign dependent. The direction of $\vec{a}$ can be reversed by forming a crossing of the perimeter line as shown in Fig. 3. When this crossing is placed at the middle of the line, perfect annihilation of the area is achieved.

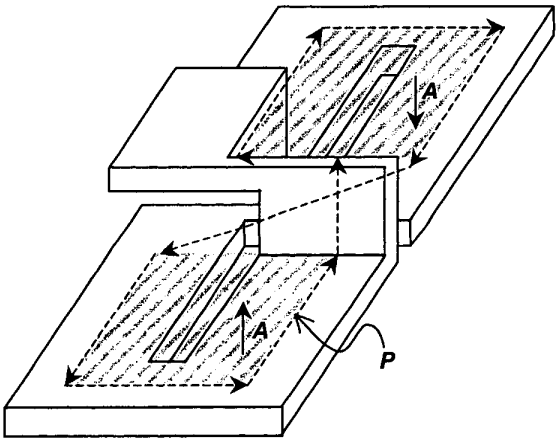


Fig. 3. Slots with crossovers create two areas with opposite clock sense.

We therefore divide a wire into N subwires and place crossovers in such a way that all left-hand side integrals of (1) between each pair of subwires vanish. This can be achieved by rotating the positions of the subwires as shown in Fig. 4, 5. Note that with this method only the inter-subwire eddy currents and not the intra-subwire eddy currents are suppressed. The width of the subwires should be chosen small enough to suppress the remaining intra-subwire eddy currents efficiently at the highest frequency of interest while avoiding excessive DC-resistance increase due to the slots, which reduce the metal-cross section when the wire width is kept constant. From here on we will abbreviate the new method with the term "interchanged subwires" (IS).

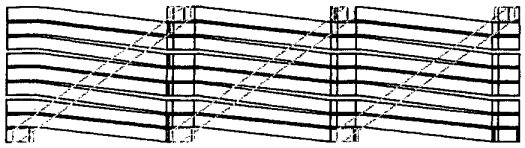


Fig. 4. Cut-out layout plot of the microstrip ground line with interchanged subwires

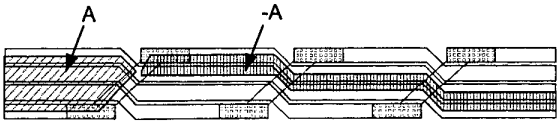


Fig. 5. Compressed layout plot of the IS signal line. Two areas of opposite orientation between two subwires are labeled

III. Test Structures

Test structures were all fabricated in an Austria Micro Systems (AMS) 0.6 µm standard CMOS process with 3 layers of metallization. The effectiveness of the suppression of conductor eddy currents is investigated by comparing two microstrip lines. One with solid metal lines and the other with IS signal line (Fig. 5) and IS ground line (Fig. 4). The signal conductor is formed by a 20 µm wide and 0.5 mm long metal 3 line while the ground line of the microstrips is formed by 94 µm wide metal 1. The oxide thickness between metal 1 and metal 3 is 1.3 µ. The bulk resistance under the ca. 15 µm thick epi layer is about 20 mΩ cm. The subwire width was chosen to be 4.3 µm. This yields a 17% higher DC-resistance for the subwire-line. The underpasses of the subwires of the signal line as well as of the ground line are formed in metal 2.

IV. Results and Discussion

Measurements were performed with a HP 8510 Network analyzer and Picoprobe GSG probe heads. Great care was taken to achieve good contacts with approx. resistance of 0.1 Ω and deembedding of the pads with an open structure.

At high frequencies, the eddy currents induced in the ground plane of a microstrip line have the tendency to cancel out the magnetic field of the signal line at the

ground-metal surface. This constricts the magnetic field in the space between signal line and ground line and reduces the inductance value until perfect constriction is achieved and current only flows on the metal surface. By using interchanged subwires, this effect is suppressed and the inductance decrease is reduced. This can clearly be seen in Fig. 6. The inductance is extracted from S-parameters using the circuit shown in the inset of Fig. 6.

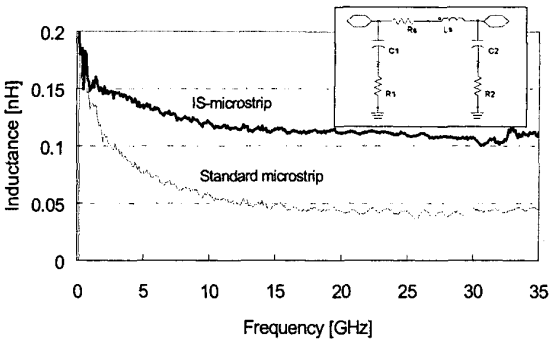
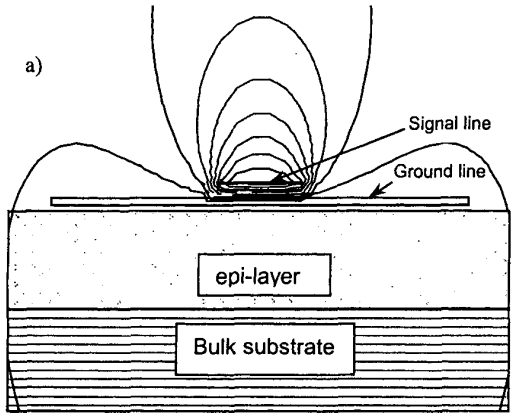


Fig. 6. Measured inductance of a standard microstrip and microstip with interchanged subwires (IS).

Fig. 7 illustrates the magnetic field distribution for the two lines at 20 GHz. In case of the standard microstrip line the magnetic field lines are nearly completely constricted between the two metal lines. In case of IS line, the magnetic field penetrates deeper into substrate. However, it does hardly reaches the low resistive bulk substrate. This means that the shielding of the magnetic field against the low resistive region is still effective.



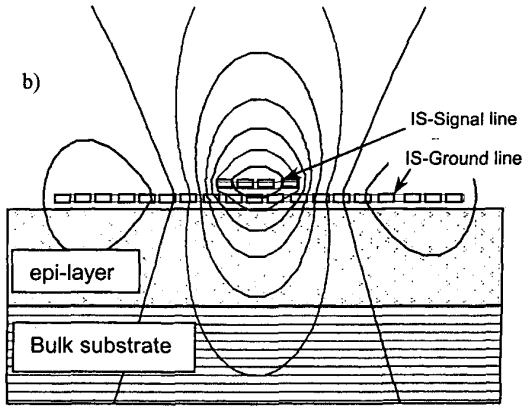


Fig. 7. Simulation of the magnetic field lines at 20 GHz for a) standard and b) IS microstrip line.

The simulations were carried out with a simulation method similar to [4]. The substrate was neglected in the calculation, which is justified by the fact that the magnetic field does only weekly penetrate into the low resistance bulk substrate.

As a result of the greater inductance of the IS-line, also the characteristic impedance of this line is higher at higher frequency as can be seen in Fig. 8. The characteristic impedance, as well as other line parameters can be extracted from S-parameters using well established methods [5]. Due to the short line lengths, we cannot exclude uncertainties in the extraction and therefore concentrate on the comparison of the two lines.

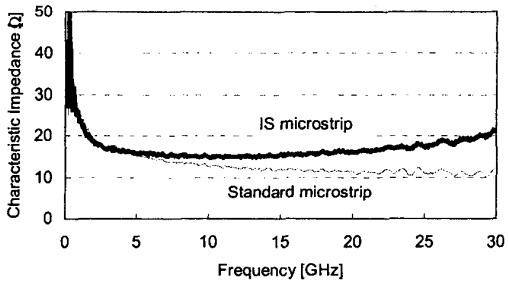


Fig. 8. Measured characteristic impedance.

Reduced eddy currents also ensure fewer losses. This can be seen in Fig. 9. The loss of the IS-microstrip line is close to being half that of the standard microstrip line around 20 GHz.

The reduced attenuation is partly due to the fact that attenuation is approximately inversely proportional to characteristic impedance, when neglecting conductance [6].

$$\alpha \approx \frac{1}{2}\frac{R}{\sqrt{\frac{L}{C}}} \propto \frac{R}{Z_0}$$

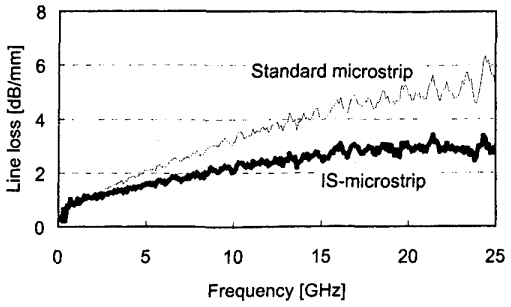


Fig. 9. Comparison of measured line loss

For typical microwave circuits the line length is rather chosen in relation to wavelength λ than to physical line length. In this case the loss per wavelength is more significant. It is plotted in Fig. 10. Because of the higher inductance of the IS-microstrip line, the wavelength of the IS-microstrip line is shorter and therefore the loss per wavelength is nearly one third to the standard microstrip line.

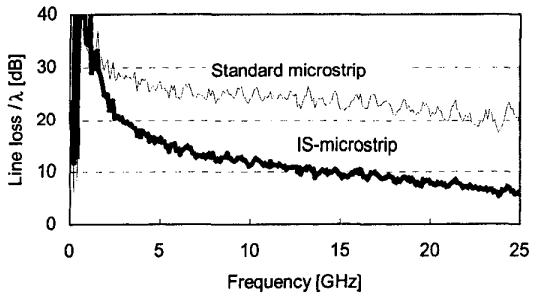


Fig. 10. Comparison of measured loss per wavelength

Although it is obvious that the IS structure is superior to the standard microstrip line, the performance suffers from the fact that only a very small oxide thickness is available in our standard CMOS process. Generally speaking, the IS method will improve high-frequency performance of all structures except those where constriction of magnetic field is desired. It is interesting to note, that the IS method becomes more effective with smaller metal spacing. This means that not only metal thickness, but also minimum feature size can improve HF performance.

Further research on the application of the IS-method for coplanar lines, on non-epi substrates and for planar inductors is under way. In all cases, higher inductance and fewer loss due to reduced conductor eddy currents is expected.

V. Conclusion

A new transmission line structure is presented that features lower loss and less frequency degradation of line parameters. This is achieved by applying a new technique for the suppression of conductor eddy currents [1]. The improvement was demonstrated with a microstrip line fabricated in a standard CMOS process with low resistance bulk substrate.

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